This listing of claims will replace all prior versions, and listings, of claims in the application:

The Status of the Claims

1. (Original) A method for manufacturing a flash memory device, the method comprising:

forming a tunnel oxide layer on a semiconductor substrate;

forming a floating gate on the tunnel oxide layer;

forming a source/drain region at both sides of the floating gate by implanting ions into the semiconductor substrate including the floating gate;

forming spacers on sidewalls of the floating gate;

depositing a sacrificial layer on the resulting substrate;

exposing some part of the substrate and the floating gate by removing some part of the sacrificial layer and the tunnel oxide layer;

forming a first trench on the exposed part of the substrate and a second trench on the exposed part of the floating gate;

depositing an oxide layer to fill the first and second trenches with the oxide layer;

removing the oxide layer and the sacrificial layer until the floating gate is exposed;

removing the spacers and the remaining sacrificial layer to form a floating gate with the second trench and a trench-type device isolation layer; and

depositing a gate insulating layer and a second polysilicon layer for a control gate on the resulting substrate.

2. (Currently Amended) A method as defined by claim 1, wherein the first polysilicon layer is formed more thickly than the ~~first trench~~ device isolation layer.

3. (Currently Amended) A method as defined by claim 2, wherein the first polysilicon layer is 300Å~2500Å thicker than the ~~first trench as a~~ device isolation layer.

4. (Original) A method as defined by claim 1, wherein the spacers are formed of nitride.

5. (Original) A method as defined by claim 1, wherein the sacrificial layer is formed of one of TEOS oxides, BPSG, PSG, and HDP oxides.

6. (Original) A method as defined by claim 1, wherein the oxide layer is formed of one of TEOS oxides, BPSG, PSG, and HDP oxides.

7. (Original) A method as defined by claim 1, wherein the oxide layer and the sacrificial layer are removed through a CMP process or an etch back process until the floating gate is exposed.

8. (Currently Amended) A method as defined by claim 1, wherein the spacers and the remaining sacrificial layer is removed through a wet etching process using phosphoric acid at a temperature higher than 70[[Å]] °C.